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VLSI APPLICATIONS **Course Code : 316340**

Programme Name/s	**: Automation and Robotics/ Digital Electronics/ Electronics & Tele-communication Engg./ Electronics & Communication Engg./ Electronics Engineering/ Industrial Electronics**
Programme Code	**: AO/ DE/ EJ/ ET/ EX/ IE**
Semester	**: Sixth**
Course Title	**: VLSI APPLICATIONS**
Course Code	**: 316340**

I. RATIONALE

VLSI (Very-Large-Scale Integration) design equips aspiring engineers with hands-on experience in both front-end and back-end processes. As a rapidly evolving technology in the industry, VLSI offers vast opportunities for innovation. This course provides students with fundamental skills to develop applications in VLSI using VHDL programming. Additionally, it enables them to utilize FPGA and ASIC chips for design and implement various applications.

II. INDUSTRY / EMPLOYER EXPECTED OUTCOME

The aim of this course is to attend following industry/employer excepted outcome through various teaching learning experiences: Develop VLSI-based electronic circuit/component using VHDL.

III. COURSE LEVEL LEARNING OUTCOMES (COS)

Students will be able to achieve & demonstrate the following COs on completion of course based learning

- CO1 - Interpret CMOS technology circuits and its applications.
- CO2 - Develop digital circuits on CPLD and FPGA devices.
- CO3 - Use VHDL to develop and test digital circuits.
- CO4 - Develop VHDL program for given application.
- CO5 - Interpret VHDL simulation and synthesis.

IV. TEACHING-LEARNING & ASSESSMENT SCHEME

Course Code	Course Title	Abbr	Course Category/s	Learning Scheme					Credits	Assessment Scheme											
				Actual Contact Hrs./Week			SLH	NLH		Paper Duration	Theory				Based on LL & TL				Based on SL		Total Marks
															Practical						
				CL	TL	LL					FA-TH	SA-TH	Total		FA-PR		SA-PR		SLA		
											Max	Max	Max	Min	Max	Min	Max	Min	Max	Min	
316340	VLSI APPLICATIONS	VLS	DSE	4	-	2	2	8	4	3	30	70	100	40	25	10	25#	10	25	10	175

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Total IKS Hrs for Sem. : Hrs
Abbreviations: CL- ClassRoom Learning , TL- Tutorial Learning, LL-Laboratory Learning, SLH-Self Learning Hours, NLH-Notional Learning Hours, FA - Formative Assessment, SA -Summative assessment, IKS - Indian Knowledge System, SLA - Self Learning Assessment
Legends: @ Internal Assessment, # External Assessment, *# On Line Examination , @$ Internal Online Examination
Note :

1. FA-TH represents average of two class tests of 30 marks each conducted during the semester.
2. If candidate is not securing minimum passing marks in FA-PR of any course then the candidate shall be declared as "Detained" in that semester.
3. If candidate is not securing minimum passing marks in SLA of any course then the candidate shall be declared as fail and will have to repeat and resubmit SLA work.
4. Notional Learning hours for the semester are (CL+LL+TL+SL)hrs.* 15 Weeks
5. 1 credit is equivalent to 30 Notional hrs.
6. * Self learning hours shall not be reflected in the Time Table.
7. * Self learning includes micro project / assignment / other activities.

V. THEORY LEARNING OUTCOMES AND ALIGNED COURSE CONTENT

Sr.No	Theory Learning Outcomes (TLO's)aligned to CO's.	Learning content mapped with Theory Learning Outcomes (TLO's) and CO's.	Suggested Learning Pedagogies.
1	TLO 1.1 Describe working of MOS transistor as a switch. TLO 1.2 Sketch the given gates using CMOS logic circuits. TLO 1.3 Explain stepwise process of CMOS fabrication. TLO 1.4 Differentiate between the nwell and pwell CMOS. TLO 1.5 Define the given specification/characteristics of CMOS logic family.	**Unit - I Introduction to CMOS Technology** 1.1 MOS Transistor: symbol, characteristics and operation, switch level modes connection, behavior of series & parallel MOS transistor switch, transmission gates and tristate logic 1.2 CMOS fabrication process: Wafer processing, oxidation, epitaxy deposition, ion-implementation, diffusion, metallization, packaging 1.3 Types of CMOS fabrication: nwell, pwell, twin tub process 1.4 Specifications of CMOS logic family: metastability, noise margins, power dissipation, fan-out, skew, figure of merits (Definitions only) and the parameter values 1.5 CMOS circuits for Boolean function	Lecture Using Chalk-Board Presentations Educational Video
2	TLO 2.1 Differentiate between Asynchronous and synchronous logic circuits with the help of suitable examples. TLO 2.2 Explain the Moore and Mealy machine design method with the help of suitable diagram and example. TLO 2.3 Describe the functions of each block of the given type of CPLD, FPGA, ASIC IC. TLO 2.4 Interpret FPGA, CPLA and ASIC parameters.	**Unit - II Advance Programmable Digital Devices (CPLD, FPGA, ASIC)** 2.1 Review of Sequential Logic circuits, comparison of Asynchronous and Synchronous 2.2 Moore and Mealy machine: block diagram, design examples on Moore and Mealy such as counter, sequence detector only 2.3 CPLD: concept, architecture, internal block diagram, applications 2.4 FPGA: concept, block diagram, architecture, applications. differentiate between FPGA and CPLD 2.5 ASIC: concept and design flow	Lecture Using Chalk-Board Presentations Flipped Classroom

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Sr.No	Theory Learning Outcomes (TLO's)aligned to CO's.	Learning content mapped with Theory Learning Outcomes (TLO's) and CO's.	Suggested Learning Pedagogies.
3	TLO 3.1 Differentiate between VHDL and Verilog on the given parameters. TLO 3.2 Optimize VHDL programming steps with its syntax. TLO 3.3 Use basic elements of VHDL programming and develop the simple code for the given function. TLO 3.4 Describe various data types used in VHDL programming with examples. TLO 3.5 Use VHDL operators to develop mathematical expressions.	**Unit - III Introduction to VLSI Design Concepts** 3.1 Hardware Description Languages (HDL): Very High-Speed HDL(VHDL) vs Verilog, and their functionality and comparison 3.2 VHDL: Features, structure and elements of VHDL (entity, architecture, configuration, package, library only definitions) 3.3 Basic Language Elements: Identifiers, VHDL objects: signal, variables and constant (syntax and use) 3.4 VHDL data types: scalar, array, composite, enumerated 3.5 VHDL operators: relational, arithmetic, logical and shift	Lecture Using Chalk-Board Educational Video Presentations
4	TLO 4.1 Compare the VHDL modelling style. TLO 4.2 Develop VHDL program using concurrent statement for the given application. TLO 4.3 Develop VHDL program using sequential statement for given application. TLO 4.4 Implement given combinational and sequential logic circuits using VHDL. TLO 4.5 Develop VHDL test bench code for the given circuit.	**Unit - IV VHDL Programming** 4.1 VHDL Modeling: data flow, behavioral, structural 4.2 Concurrent constructs (when, with) 4.3 Sequential constructs (process, if, case, loop, assert, wait) 4.4 VHDL code for combinational circuits – Logic gates, adder, subtractor, multiplexer, demultiplexer, encoder, decoder, comparator, 4-bit ALU 4.5 VHDL code for Sequential circuits – D, T and JK flip-flop, 4 bit up/down counter, MOD counter, shift registers (4-bit SISO and PIPO) 4.6 Test bench: simple test bench for a combinational circuit (full adder) and sequential logic circuit (D/T flipflop)	Lecture Using Chalk-Board Educational Video Collaborative learning
5	TLO 5.1 Describe the features of the given type of simulator with a suitable example. TLO 5.2 Define the given component in HDL simulation process. TLO 5.3 Prepare flowchart for the HDL design synthesis process. TLO 5.4 Summarize stepwise HDL design flow.	**Unit - V HDL Simulation and Synthesis** 5.1 Types of simulators: event based and cycle based 5.2 Components: Event scheduling, sensitivity list, zero modelling, simulation cycle 5.3 HDL synthesis process: Boolean optimization, flattering, factoring, mapping to gates 5.4 HDL Design flow: RTL simulation, gate-level verification, place and route	Lecture Using Chalk-Board Flipped Classroom Educational Video

VI. LABORATORY LEARNING OUTCOME AND ALIGNED PRACTICAL / TUTORIAL EXPERIENCES.

Practical / Tutorial / Laboratory Learning Outcome (LLO)	Sr No	Laboratory Experiment / Practical Titles / Tutorial Titles	Number of hrs.	Relevant COs
LLO 1.1 Identify various blocks of FPGA and CPLD. LLO 1.2 Test the functionality of various pins of FPGA and CPLD.	1	*Identification of internal block and pin configuration of FPGA & CPLD	2	CO2

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Practical / Tutorial / Laboratory Learning Outcome (LLO)	Sr No	Laboratory Experiment / Practical Titles / Tutorial Titles	Number of hrs.	Relevant COs
LLO 2.1 Install relevant EDA (such as Xilinx software) tool for VHDL. LLO 2.2 Check the VHDL libraries installed in VHDL environment.	2	*Installation of EDA tool and the relevant libraries for VLSI code development	2	CO3
LLO 3.1 Test the functionality of basic logic gates using VHDL Data flow model. LLO 3.2 Test the functionality of universal logic gates using VHDL Data flow model.	3	*Develop VHDL code for basic and universal gate for data flow model	2	CO3
LLO 4.1 Test the functionality of basic logic gates using VHDL behavioral model. LLO 4.2 Test the functionality of universal logic gate using VHDL behavioral model.	4	Develop VHDL code for basic and universal gate for behavioral model	2	CO3
LLO 5.1 Test the functionality of half and full adder using VHDL code. LLO 5.2 Test the simulated Test bench waveform.	5	*Realize the half and full Adder on FPGA board	2	CO3
LLO 6.1 Test the functionality of 4:1 multiplexer using VHDL code.	6	*Realize the Multiplexer on FPGA board	2	CO3
LLO 7.1 Test the functionality of 1:8 De-multiplexer using VHDL code.	7	Realize the De-multiplexer on FPGA board	2	CO3
LLO 8.1 Interpret the output of 4:2 encoder using VHDL code.	8	Design 4:2 encoder on FPGA board	2	CO3
LLO 9.1 Interpret the output of 3:8 decoder using VHDL code.	9	Design 3:8 decoder on FPGA board	2	CO3
LLO 10.1 Test the functionality of D flipflop using VHDL code. LLO 10.2 Test the functionality of T flipflop using VHDL code.	10	*Realize the D and T flipflop on FPGA board	2	CO3
LLO 11.1 Test the functionality of 2-bit comparator using VHDL code.	11	Design Comparator on FPGA board	2	CO3
LLO 12.1 Interpret the output of Mod-10 Up counter using VHDL code.	12	Design Up Counter on FPGA board	2	CO3
LLO 13.1 Develop VHDL code for 4-bit Up/Down Synchronous counter and test the circuit on FPGA board..	13	Design Synchronous counter on FPGA board	2	CO3
LLO 14.1 Test the functionality of 4-bit binary to gray code converter & Synthesize using FPGA.	14	Design binary to gray code converter circuit using FPGA board	2	CO3
LLO 15.1 Develop VHDL code for 8-bit Digital to analog converter (DAC) & test the circuit on FPGA board	15	*Design digital to analog converter (DAC) using FPGA board	2	CO4
LLO 16.1 Optimize the VHDL code to rotate stepper motor in clockwise direction.	16	*Design stepper motor Controller using FPGA board	2	CO5
LLO 17.1 Develop VHDL code for 4-bit ALU and simulate it using FPGA.	17	Design of 4-bit ALU/ sequence detector using FPGA board	2	CO5

Note : Out of above suggestive LLOs -

- '*' Marked Practicals (LLOs) Are mandatory.
- Minimum 80% of above list of lab experiment are to be performed.
- Judicial mix of LLOs are to be performed to achieve desired outcomes.

VII. SUGGESTED MICRO PROJECT / ASSIGNMENT/ ACTIVITIES FOR SPECIFIC LEARNING / SKILLS DEVELOPMENT (SELF LEARNING)

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Assignment

- Develop the flowchart for simulation used in VHDL.
- Write syntax for concurrent and sequential statements.
- Write test bench code of universal shift register using VHDL.
- Describe architecture of CPLD/FPGA with function of each block.
- Develop flow chart of CMOS IC fabrication in p-well and n-well process.

Micro project

- Build a small ASIC system for your Home /Community.
- Develop four-bit addition/subtraction circuit using VHDL code.
- Develop square wave generator system of frequency = 1 Hz/100Hz
- Develop a VLSI based alarm system when a customer enters into the shop through exits door.
- Build a VLSI based system for vehicle security system.
- Design traffic light system using CPLD/FPGA.
- Design Lift controller system using CPLD/FPGA.

Note :

- Above is just a suggestive list of microprojects and assignments; faculty must prepare their own bank of microprojects, assignments, and activities in a similar way.
- The faculty must allocate judicial mix of tasks, considering the weaknesses and / strengths of the student in acquiring the desired skills.
- If a microproject is assigned, it is expected to be completed as a group activity.
- SLA marks shall be awarded as per the continuous assessment record.
- For courses with no SLA component the list of suggestive microprojects / assignments/ activities are optional, faculty may encourage students to perform these tasks for enhanced learning experiences.
- If the course does not have associated SLA component, above suggestive listings is applicable to Tutorials and maybe considered for FA-PR evaluations.

VIII. LABORATORY EQUIPMENT / INSTRUMENTS / TOOLS / SOFTWARE REQUIRED

Sr.No	Equipment Name with Broad Specifications	Relevant LLO Number
1	VLSI trainer kit along with DAC/ADC trainer kit.	15
2	VLSI trainer kit along with stepper motor.	16
3	FPGA trainer kit with Accessories	2,4,5,6,7,8,9,10,11,12,13,14,15,16,17
4	JTAG cable, DMM, Bread board.	3,4,5,6,7,8,9,10,11,12,13,14,15,16,17
5	VLSI trainer kit with accessories such as switches,LED,seven segment display etc.	4,5,6,7,8,9,10,11,12,13,14,15
6	Personal computer with latest configuration.	All

IX. SUGGESTED WEIGHTAGE TO LEARNING EFFORTS & ASSESSMENT PURPOSE (Specification Table)

Sr.No	Unit	Unit Title	Aligned COs	Learning Hours	R-Level	U-Level	A-Level	Total Marks
1	I	Introduction to CMOS Technology	CO1	12	2	4	8	14
2	II	Advance Programmable Digital Devices (CPLD, FPGA, ASIC)	CO2	10	2	2	6	10
3	III	Introduction to VLSI Design Concepts	CO3	14	4	4	8	16
4	IV	VHDL Programming	CO4	16	4	6	10	20
5	V	HDL Simulation and Synthesis	CO5	8	2	2	6	10
Grand Total				**60**	**14**	**18**	**38**	**70**

X. ASSESSMENT METHODOLOGIES/TOOLS

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Formative assessment (Assessment for Learning)

- Two offline unit test of 30 marks and average of two-unit test will considered for out of 30 marks.
- For formative assessment of laboratory learning 25 marks.
- Each practical will be assessed considering 60% weightage to process, 40% weightage to product.

Summative Assessment (Assessment of Learning)

- End semester assessment of 70 marks.
- End semester summative assessment of 25 marks for laboratory learning.

XI. SUGGESTED COS - POS MATRIX FORM

Course Outcomes (COs)	Programme Outcomes (POs)							Programme Specific Outcomes* (PSOs)		
	PO-1 Basic and Discipline Specific Knowledge	PO-2 Problem Analysis	PO-3 Design/ Development of Solutions	PO-4 Engineering Tools	PO-5 Engineering Practices for Society, Sustainability and Environment	PO-6 Project Management	PO-7 Life Long Learning	PSO-1	PSO-2	PSO-3
CO1	3	1	1	1	1	1	2			
CO2	3	2	1	1	1	1	2			
CO3	3	2	2	2	2	2	3			
CO4	3	3	3	3	2	2	3			
CO5	3	3	3	2	2	2	3			

Legends :- High:03, Medium:02,Low:01, No Mapping: -
*PSOs are to be formulated at institute level

XII. SUGGESTED LEARNING MATERIALS / BOOKS

Sr.No	Author	Title	Publisher with ISBN Number
1	Gaganpreet Kaur	VHDL Basics to programming	Pearson Education India, 2011 ISBN: 9788131732113
2	John M. Yarbrough	Digital Logic: Application and Design	C.L Engineering, ISBN: 978 034066756
3	Willian I. Fletcher	An Engineering approach to digital design	Prentice- Hall of India ISBN: 9780132776998
4	Douglas Perry	VHDL programming by example	Tata McGraw-Hill ISBN: 9780070499447
5	Eugene D. Fabricius	Introduction to VLSI Design	McGraw Hill ISBN:9780070199484
6	Sarkar & Sarkar	VLSI design and EDA tools	Scitech Publications (lndia) Pvt Ltd ISBN: 9788183714976

XIII . LEARNING WEBSITES & PORTALS

Sr.No	Link / Portal	Description
1	https://docs.amd.com/v/u/en-US/ug1655-ise-documentation	ISE documentation for version 14.7
2	https://web.eecs.utk.edu/~dbouldin/protected/xilinx-ise-quick-start.pdf	ISE quick start tutorial
3	https://www.allaboutelectronics.org/cmos-logic-gates-explained/	Logic gates implementation using CMOS inverter

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Sr.No	Link / Portal	Description
4	https://www.geeksforgeeks.org/vhdl-very-high-speed-integrated-circuit-hardware-description-language/	VHDL programming.
5	https://nptel.ac.in/courses/117106092	NPTEL- VLSI Design Course

Note :

- Teachers are requested to check the creative common license status/financial implications of the suggested online educational resources before use by the students

MSBTE Approval Dt. 04/09/2025 **Semester - 6, K Scheme**